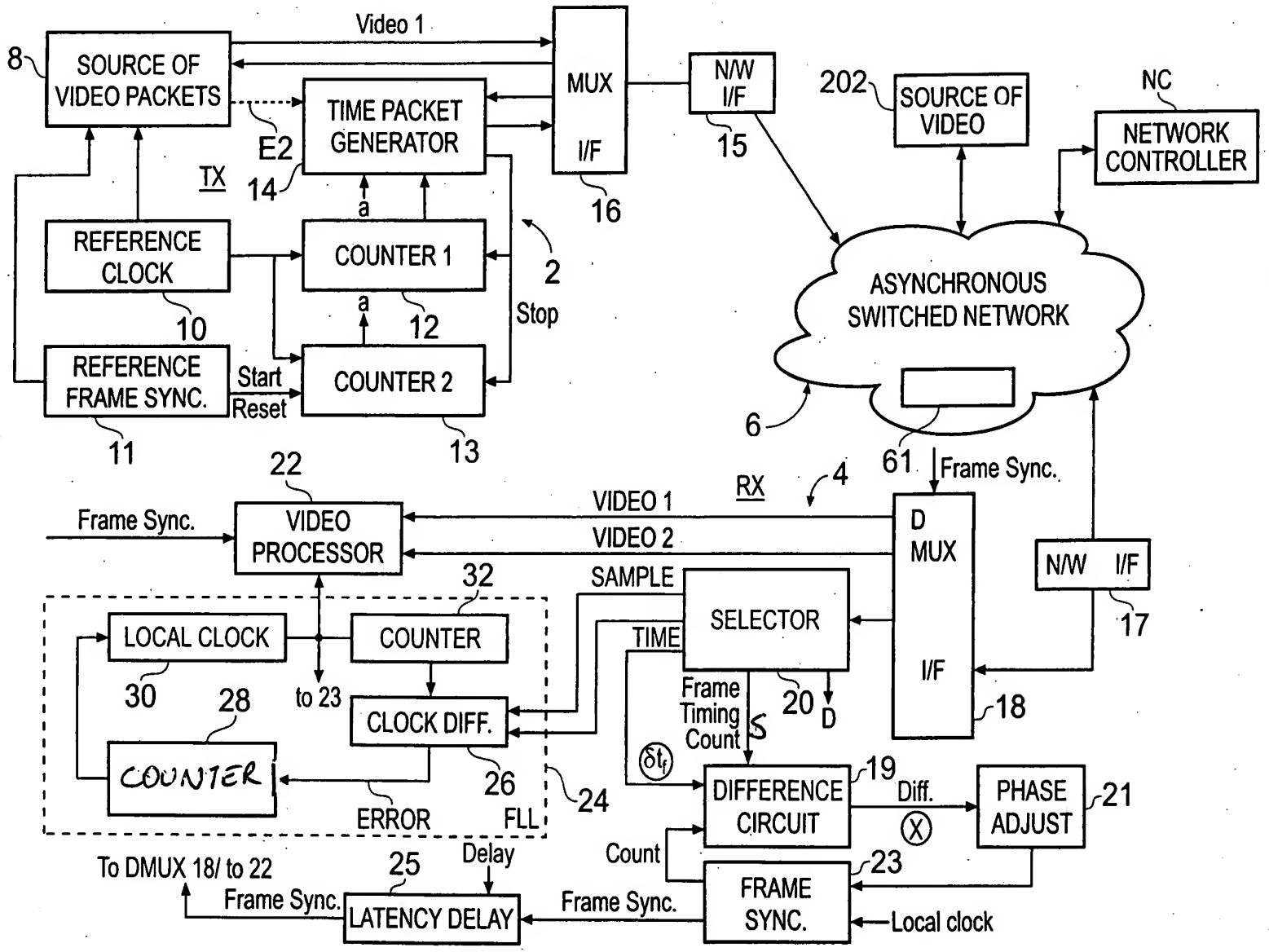
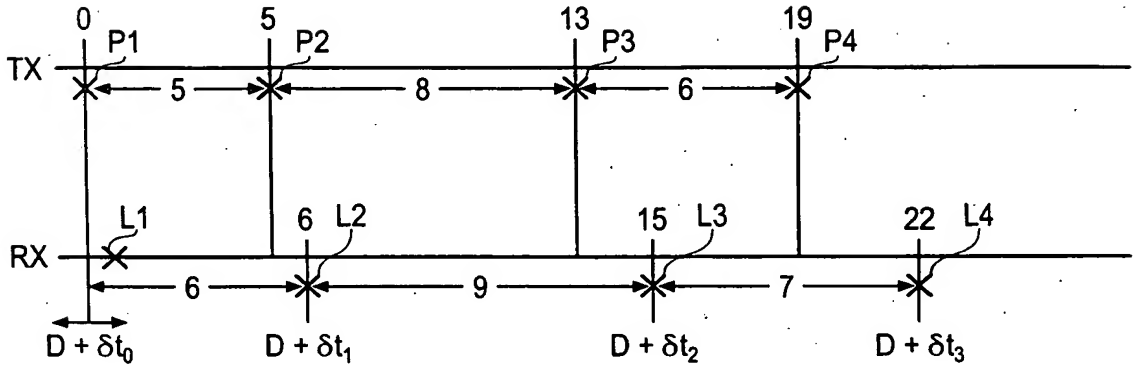


Fig. 1



Second, RX, diff.	6	9	7
First, TX, diff.	5	8	6
Error	1	1	1
Cumulative Error	1	2	3

Fig. 2

Ethernet Frame Header	IP Datagram Header	UDP Header	Time stamp Data	Frame Timing Data	CRC

Fig. 3: UDP Timing Packet

Ethernet Frame Header	IP Datagram Header	UDP Header	Video Data	CRC

Fig. 7: Video Packet

Ethernet Frame Header	IP Datagram Header	UDP Header	Timestamp Data	Frame Timing Data	Video Data	CRC

Fig. 8: Combined Packet

Ethernet Frame Header	IP Datagram Header	UDP Header	Frame Timing Data	CRC

Fig. 9: UDP Frame Timing Packet

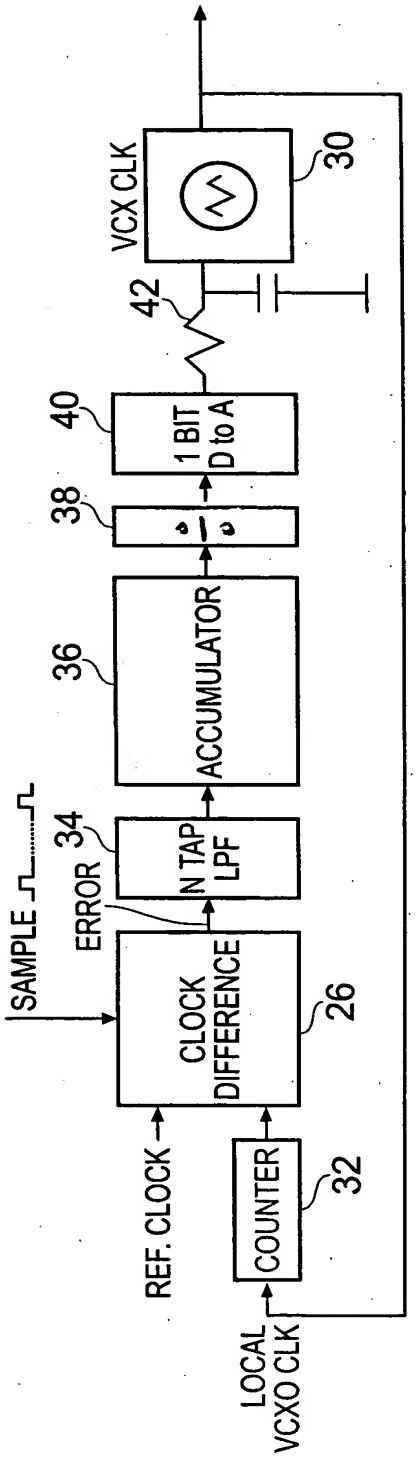


Fig. 4: Frequency Locking System

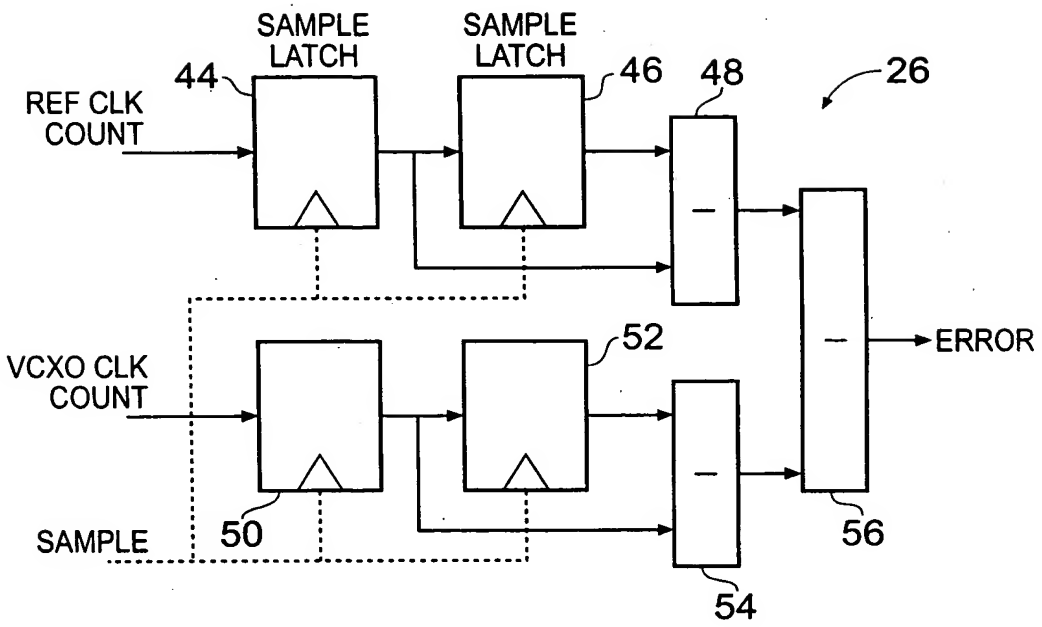


Fig. 5: Clock Difference Circuit

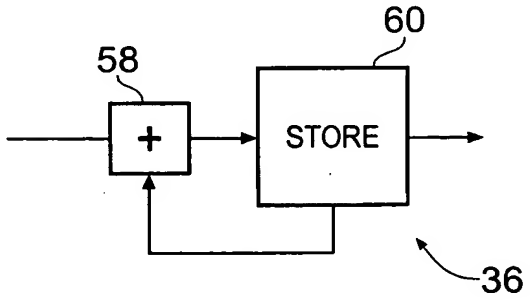


Fig. 6: Accumulator

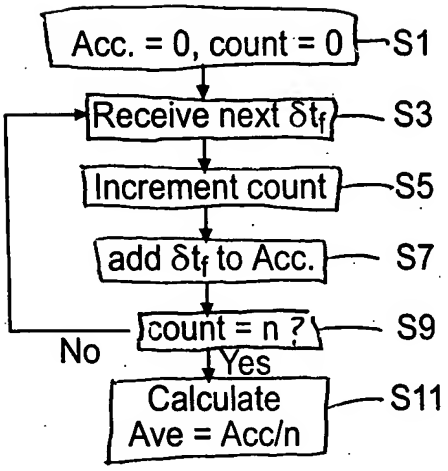

Acc. = 0, count = 0
S1
Receive next δtf
S3
Increment count
S5
add δtf to Acc.
S7
count = n ?
S9
No
Yes
Calculate
Ave = Acc/n
S11

Fig. 11

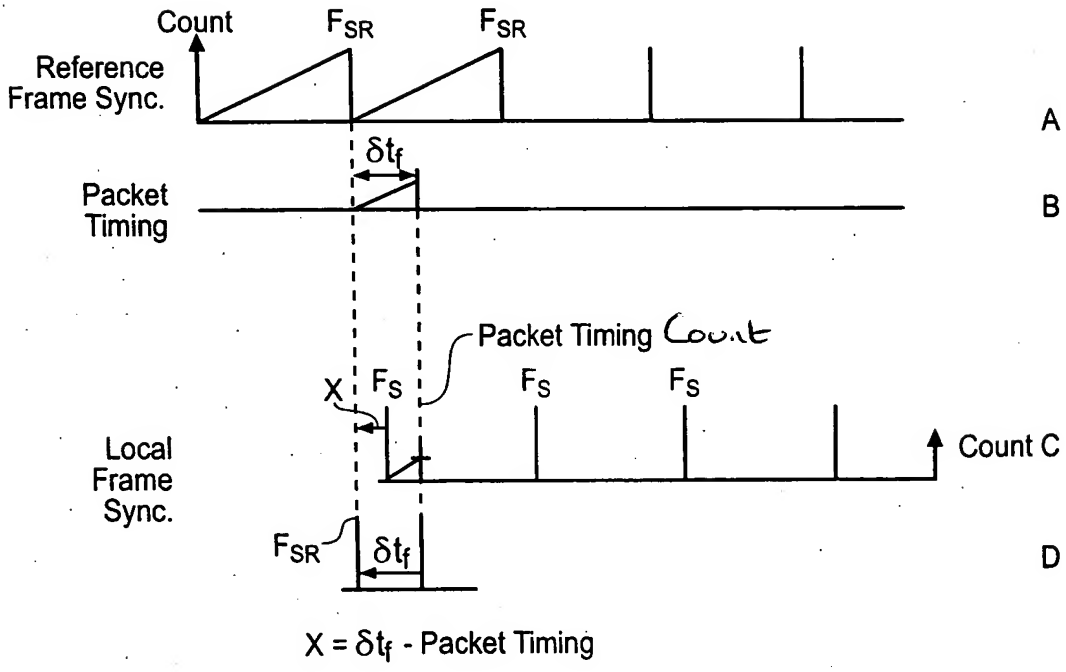

Count
FSR
FSR
Reference
Frame Sync.
A
δtf
Packet
Timing
B
Packet Timing Count
X
FS
FS
FS
Local
Frame
Sync.
Count C
FSR
δtf
D
X = δtf - Packet Timing

Fig. 10

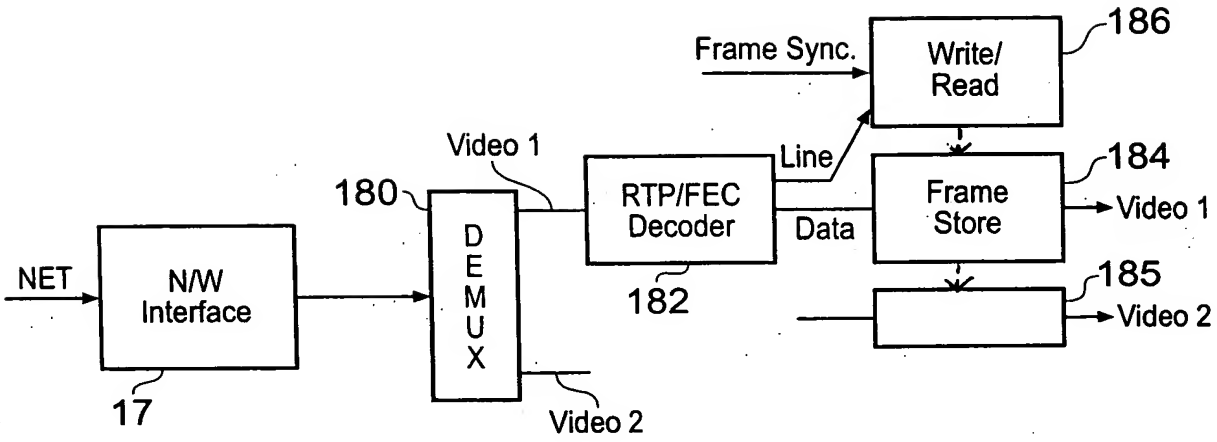

Frame Sync.
Write/
Read
186
Video 1
180
DEMUX
RTP/FEC
Decoder
Line
Data
184
Frame
Store
Video 1
NET
N/W
Interface
182
185
Video 2
17
Video 2

Fig. 12

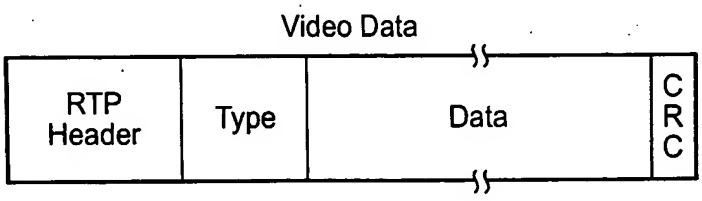

Video Data
RTP
Header
Type
Data
CRC

Fig. 13